



IEEE Joint Huntsville Section & JCAM Meeting



- Speaker:** Dr. Gerry Cain, DSP Creations, Ltd.
- Subject:** Easing DSP Algorithm Development for Communications
- Date:** Monday, August 8th, 2005
- Time:** 11:15am - 1:00pm
- Place:** UAH Engineering Building, Conference Room 258
- Reservations:** Please contact Sonya Hutchinson at 544-3312, if you plan to attend. You may also email her at: Sonya.L.Hutchinson@nasa.gov.

Biographical Sketch: Dr. Gerry Cain is currently a Director of two companies: Signalytics (a training company) and DSP Creations Limited (a DSP software firm) and has in-depth experience in the Digital Signal Processing area, both in industrial and university teaching and research settings.

Dr. Cain was with Sandia National Laboratories in Albuquerque, refining early laser radars and developing test range timing and control instrumentation prior to joining Teledyne Brown Engineering Company at Huntsville, Alabama, where he led a small team of radar analysts. He later was Professor of DSP and Head of the School of Electronic & Manufacturing Systems Engineering at the University of Westminster in London. He recently spent a two-year period with The MathWorks Limited at Cambridge, England, as Business Manager for DSP and Communications.

Abstract: Modern communication systems are growing in complexity, with ever-tighter interdependence of modulation, coding, detection and signal enhancement schemes. Multi-Carrier Modulation, spread-spectrum CDMA, and now Ultra-Wideband scenarios are competing, clashing and cross-fertilizing at an alarming tempo. DSP algorithms fuel this diversity of burgeoning approaches, but the sophisticated frameworks laid down in advance for overall systems makes innovation in algorithms cumbersome.

It is far too late – once an entire system is shaping up – to commence major revision of the underlying algorithms being employed for such tasks as frequency estimation, channel estimation, synchronization or equalization. Proof-of-Concept experimentation needs to be done early; while re-thinking is cheap and detailed processing techniques are not yet entrenched.

The tools described in this talk make it easy to quickly assemble the key elements of new DSP algorithms and rapidly gain insight into their feasibility and effectiveness. This is done at graphical block diagram level, without the necessity of any code-writing burden, by use of a special Simulink-based LabKit. Within a few short minutes the essence of a processing subsystem can be wired-up (virtually), flexibly exercised and visually monitored on powerful Signal Analyzers.

Notes: You do not have to be an IEEE member to attend. All guests are welcome. We will eat from 11:15 - 11:45am and the talk will begin at 11:45am. We will be ordering Quizno's to be delivered to the conference room. Please call Sonya by 7/5/05 to order your lunch. Cost subject to food selection. See menu at: <http://www.quiznos.com/menu.asp>



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